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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,641	01/18/2001	Shunpei Yamazaki	740756-002249	6097
22204	7590	06/16/2005	EXAMINER	
NIXON PEABODY, LLP			BOOTH, RICHARD A	
401 9TH STREET, NW				
SUITE 900			ART UNIT	
WASHINGTON, DC 20004-2128			2812	
			PAPER NUMBER	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

fm

Office Action Summary	Application No.		Applicant(s)	
	09/761,641		YAMAZAKI ET AL.	
	Examiner		Art Unit	
	Richard A. Booth		2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6/3/05.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 6-14 and 19-48 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6-14 and 19-48 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 6-14, and 19-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki, U.S. Patent 4,727,044 in view of Silver, U.S. Patent 5,104,818 and further in view of Chang, U.S. Patent 5,064,775, Zhang et al., U.S. Patent 5,904,509, and Miyasaka, U.S. Patent 6,455,360..

Yamazaki shows the invention substantially as claimed including forming a semiconductor film 2 having an amorphous structure over a substrate 1; crystallizing the semiconductor film (see col. 6-lines 49-55), and wherein a concentration of carbon,

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nitrogen, and oxygen are present in an amount less than 5×10^{18} atoms/cm³ (see col. 8-lines 18-20).

Yamazaki fails to expressly disclose ion-doping an impurity element into a channel region, wherein said impurity element imparts p-type conductivity to said semiconductor film, wherein the concentration of said impurity element is 2×10^{17} atoms/cm³ after the step.

Silver shows the invention substantially as claimed including a method of manufacturing a semiconductor device comprising: ion-doping an impurity element into a channel region, wherein said impurity element imparts p-type conductivity to said semiconductor film (see fig. 1C), wherein the concentration of said impurity element is 2×10^{17} atoms/cm³ after the step (see figs. 1c-1f and col. 2-lines 29-54). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki so as to implant the channel region as shown by Silver because such an implant is an effective way to control the threshold voltage of the transistor.

Yamazaki and Silver fail to expressly disclose ion-doping an impurity element into a channel region of the semiconductor film through the insulating film, with no mass separation performed in the ion-doping step and wherein said impurity element is doped by employing a source material gas comprising an impurity element diluted with hydrogen at a concentration of 0.5 to 5 percent.

Chang discloses introducing boron 36 into a semiconductor film so that the boron implanted region becomes part of a channel region (see fig. 2 and col. 4-line 55 to col.

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5-line 37), In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki modified by Silver so as to implant boron into the channel region because this will allow for more independent control of the threshold voltage. Furthermore, Zhang et al. discloses performing plasma doping without mass separation and implanting these ions into a semiconductor film through an insulating film (see col. 8-line 59 to col. 9-line 2). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki modified by Silver and Chang so as to conduct the implantation using plasma doping since plasma doping is shown to be a suitable method of injecting ions into a semiconductor. Moreover, Miyasaka discloses performing a doping step using diborane diluted with hydrogen at a concentration of 0.1 to 10% (see col. 22-lines 37-41). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki modified by Silver, Chang, and Zhang et al. so as to include a diborane gas diluted with hydrogen because Miyasaka shows this to be a suitable combination to form doped region in thin film structures.

Regarding the doping gases being used, official notice was taken regarding this fact in the office action mailed 10-10-02, and therefore this limitation is taken to be admitted prior art.

Claims 44-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki, U.S. Patent 4,727,044 in view of Silver, U.S. Patent 5,104,818 and further in

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view of Chang, U.S. Patent 5,064,775, Zhang et al., U.S. Patent 5,904,509, and Miyasaka, U.S. Patent 6,455,360. as applied to claims 1-3, 6-14, and 19-43 above, and further in view of Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology".

Yamazaki, Silver, Chang, Zhang et al., and Miyasaka are applied as above but do not expressly disclose wherein said ion-doping is performed through the insulating film. Wolf et al. discloses that commonly in order to reduce damage to the semiconductor surface, layers are deliberately added, for instance, silicon oxide layers (see page 323, "Implanting Through Surface Layers"). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform ion doping through an insulating film because this will reduce the damage to the substrate.

Response to Arguments


Applicant's arguments with respect to claims 1-3, 6-14, and 19-48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Richard A. Booth
Primary Examiner
Art Unit 2812

June 11, 2005